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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/720,030 | 11/24/2003 | Taketo Heishi | 67471-030 | 5444 |

7590 07/21/2008

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| EXAMINER | |
|---|---|
| PAN, DANIEL H | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2183 | |

| MAIL DATE | DELIVERY MODE |
|---|---|
| 07/21/2008 | PAPER |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/720,030 | HEISHI ET AL. | |
| | Examiner | Art Unit | |
| | Daniel Pan | 2183 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *27 March 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-33 and 40-54* is/are pending in the application.

4a) Of the above claim(s) *34-39* is/are withdrawn from consideration.

5)☒ Claim(s) *1-33* is/are allowed.

6)☒ Claim(s) *40-54* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *11/20/06,11/24/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

1. Claims 1-33 are original claims and remain allowed. Claims 34-39 have been canceled. Claims 1-33 ,40-54 remain for examination.

2. Claims 1-33 are allowable for the combined details of the target processor and the assignment unit (claims 1,12,18,28), the detailed fictional elements of the processor and the opcode and the unit fields of the operand of the long instruction (claims 11,27), the combined detailed features of the register set,.the decoding unit, the operation execution unit, the s+k-1 registers ,and the decoding unit (claim 24).

3. Upon further review, this action includes new objection. Therefore, this is a non-final action in order to allow applicant a chance for response. The response to applicant's remarks will be included in this action.

4. Claims 40 is objected to because of the following informalities: The language "capable" is not clear. It is confusing, and may render claim indefinite. Suggestions : "executing", "executed". Appropriate correction is required.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 40-54 are rejected under 35 U.S.C. 102(b) as being anticipated by Sato et al. (5,488,710).

6. As to newly amended feature of wherein the decoding unit is capable of decoding a pluralit3, of instructions executed in parallel. decoding unit is capable of decoding a pluralit3, of instructions executed in parallel (see execution unit and decoding unit in co1.6, lines 16-54, see also in fig.9c and in co1.8, lines 3-52 alternative embodiment for the simultaneous execution of instructions).

7. Applicant's response on 03/27/08 has been fully considered but is not persuasive.

8. In the remarks applicant argued that :

a) Sato's bus width as being 16 bits to be shorter than 16*4 = 64 bits, however, element 221 is merely one part of a decoder made up of elements 221,222,223,224,231,232,233,234 collectively; Sato does not disclose the total bit width of the instruction bus shorter than M*N bits.

9. As to a) above, examiner would like to point out that applicant only recites "an instruction bus formed between...wherein the total bit width of the instruction bus is shorter than M*N bits (see claim 40, lines 11-12). Therefore, the bus connection to each decoder is "an instruction bus" since each decoder ahs a separate instruction latch (see fig.6 [211]). And, since Sato's bus width as being 16 bits, it is shorter than 16*4 = 64 bits.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 571 272 4172. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 571 272 4162. The fax phone number for the organization where this application or proceeding is assigned is 703 306 5404.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

*21 Century Strategic Plan*

/Daniel Pan/
Primary Examiner, Art Unit 2183